III. AMENDMENTS TO THE CLAIMS:

Please accept amendment(s) to the claims as follows:

1. (Currently amended) A semiconductor comprising:

a contact having a portion that extends on two opposing vertical sides of at least one vertical structure adjacent a gate electrode, and wherein the contact contacts only one of the gate electrode and a diffusion adjacent the gate electrode.

Claims 2-3 (cancelled)

4. (Original) The semiconductor of claim 1, wherein the contact includes an upper portion that is larger than a lower, contact portion.

Claims 5-20 (Cancelled).

21. (Currently amended) The semiconductor of claim 1, wherein ~~each~~ the at least one vertical structure is a spacer.

22. (Currently amended) The semiconductor of claim 21, wherein the contact contacts a substrate adjacent ~~one~~ the spacer.

23. (Previously added) The semiconductor of claim 1, wherein the at least one vertical structure includes two vertical structures, one to each side of the gate electrode.

24. (Previously Added) The semiconductor of 23, wherein each vertical structure is a spacer.

Claims 25-33 (Cancelled).

Cnted

34. (New) A semiconductor comprising:

a gate electrode;

a spacer adjacent the gate electrode;

a contact having a portion that extends on two opposing vertical sides of the spacer, wherein the contact contacts a diffusion adjacent the gate electrode; and

a masking layer insulating the gate electrode from the contact.

35. (New) The semiconductor of claim 34, wherein the masking layer caps at least a portion of the gate electrode.

36. (New) The semiconductor of claim 34, wherein the contact has an upper portion that is larger than a lower portion that contacts the diffusion.

37. (New) The semiconductor of claim 34, wherein the contact has a portion that extends on two opposing vertical sides of the spacer.

38. (New) A semiconductor comprising:

a gate electrode;

a spacer adjacent the gate electrode;

a contact having a portion that extends on two opposing vertical sides of the spacer, wherein the contact contacts the gate electrode; and

a masking layer insulating a diffusion from the contact.

39. (New) The semiconductor of claim 38, wherein the entire contact extends on two opposing vertical sides of the spacer.

40. (New) The semiconductor of claim 39, wherein the masking layer extends about the spacer.

41. (New) The semiconductor of claim 38, wherein the contact has a lower portion that contacts the whole upper side of the gate electrode.

42. (New) The semiconductor of claim 38, wherein a contact has an upper portion larger than a lower portion that contacts the gate electrode.